

## REMARKS

Applicant has amended claims 1-36 and has added new claims 37-40.

Applicant has included an appendix which shows the amendments made to claims 1-36.

- 5           Should the examiner have any questions he is invited to call Applicant's attorney at the number given below.

Respectfully submitted,



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David G. Rasmussen

Attorney for Applicant

Reg. No. 26795

Telephone: (508) 497-0132

David G. Rasmussen

- 15   Attorney at Law

8 Hazel Rd.

Hopkinton, MA 01748



Appendix of Amendments Made to Claims 1-36

1. ~~A CMOS~~ An image sensor comprising;

a plurality of ~~active~~ pixels each having an output, each ~~active~~ pixel including;

5 a first circuit that produces a signal proportional to incident light intensity, said first circuit being connected to supply said proportional signal ~~capable of being applied to said active-pixel output,~~

a select node connected to receive a select signal for selecting  
10 said pixel from said plurality of pixels, and

a reset transistor for resetting said ~~active~~ pixel;

~~at least one select signal coupled to said pixels for selecting at least one pixel from said plurality of pixels,~~

an amplifier- having;

a first input for receiving said outputs of said ~~active~~ pixels, and

15 an output coupled to said reset transistors ~~to providing~~ provide a negative feedback signal to said a selected pixel; and

a reset reference voltage source connected to apply a reset reference voltage signal ~~applied to said amplifier to provide a voltage reference for controlling to reset~~  
20 of said active pixels.

2. The ~~CMOS~~ image sensor of claim 1 ~~in which~~ wherein said amplifier further includes a second input receiving said reset reference voltage signal.

3. The ~~CMOS~~ image sensor of claim 2 ~~in which~~ wherein said reset transistor ~~has~~  
25 includes a gate and first and second terminals, said first terminal connected to receive said negative feedback signal ~~provided to said first terminal to adjust the voltage at said second terminal's voltage of said reset transistor to a selected reset voltage.~~

4. The CMOS image sensor of claim 1 or 3 ~~in which~~ wherein said reset reference voltage source signal is selected to control said voltage at said second reset transistor terminal is to be about  $V_T - \Delta V$  below the a reset voltage applied at said gate terminal  
5 of said reset transistor, where ~~where~~  $V_T$  is ~~the a~~ a threshold voltage that is characteristic of said reset transistor, and  $\Delta V$  ~~keeps~~ is selected to maintain the said reset transistor in a the-subthreshold region of operation during in the a steady state phase of the pixel reset phase.

10 5. The CMOS image sensor of claim 4 ~~in which~~ wherein said selected  $\Delta V$  is greater than about one hundred millivolts.

6. The CMOS image sensor of claim 4 ~~in which~~ wherein each said select node of each said pixel further comprises a terminal of a row select transistor that is coupled  
15 to said first input of said amplifier.

7. The CMOS image sensor of claim 6 wherein each said pixel further comprises having a source follower transistor coupled between said second terminal of said reset transistor and a terminal of said row select transistor.

20 8. The CMOS image sensor of claim 3 ~~in which~~ wherein said first circuit is comprises a photocircuit.

9. The CMOS image sensor of claim 8 ~~in which~~ wherein said amplifier is comprises a differential amplifier including in which said first input of said differential amplifier is applied to a first differential amplifier input transistor connected to receive said first amplifier input and said second input of said  
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~~differential amplifier is applied to~~ a second differential amplifier input transistor  
connected to receive said second amplifier input, said first and second differential  
amplifier input transistors connected cooperating to provide a ~~current~~ signal to a  
current mirror circuit that is which provides connected to deliver said negative  
5 feedback signal to said reset transistor first terminal.

10. The CMOS-image sensor of claim 8 ~~in which~~ wherein said photocircuit  
includes a photodiode and a capacitance.

10 11. The CMOS-image sensor of claim 7 ~~in which~~ wherein said first circuit is a  
photocircuit.

12. The CMOS-image sensor of claim 11 ~~in which~~ wherein said photocircuit  
includes a photodiode and a capacitance.

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13. ~~A CMOS~~ An image sensor array having rows and columns of ~~active~~ pixels,  
comprising;

~~one or more~~ at least one column lines;

~~multiple~~ a plurality of ~~active~~ pixels each having an output, the outputs of ~~each~~  
20 ~~active~~ pixels in a column being connected to a common respective column line, each  
said ~~active~~ pixel including;

a first circuit that produces a signal proportional to incident light  
intensity, said first circuit being connected to supply said proportional  
signal ~~capable of being applied to~~ said ~~active~~ pixel output, and

25

a reset transistor for resetting said ~~active~~ pixel;

~~one or more~~ at least one amplifiers, each said amplifier having a first input  
coupled to at least one ~~each~~ said column line, each said amplifier being connected to

~~providing~~ provide a negative feedback signal to each said pixel reset transistor of said a respective column of pixels; and

5        -a reset reference voltage source connected to apply a reset reference voltage signal applied to each said amplifier to provide a voltage reference for controlling to reset of said active-pixels-.

14.    The CMOS-image sensor of claim 13 ~~in which~~ wherein said amplifier further includes a second input for receiving said reset reference voltage signal.

10    15.   The CMOS-image sensor of claim 14 ~~in which~~ wherein said reset transistor ~~has~~ includes a gate and first and second terminals, said first terminal connected to receive said negative feedback signal provided to said first terminal to adjust the voltage at said second terminal's voltage of said reset transistor to a selected reset voltage.

15    16.   The CMOS-image sensor of claim 13 ~~or 15 in which~~ wherein said reset reference voltage source signal is selected to control said voltage -at each- said second reset transistor terminal is to be about  $V_T - \Delta V$  below the a reset voltage applied at said gate terminal of said reset transistor, where  $V_T$  is the a threshold voltage that is characteristic of said reset transistor, and  $\Delta V$  keeps-is selected to maintain said reset  
20    transistor ~~in the a subthreshold region of operation during a in the steady state phase of the pixel reset phase.~~

17.    The CMOS-image sensor array of claim 15 ~~in which~~ wherein said selected  $\Delta V$  is greater than about one hundred millivolts.

18. The CMOS-image sensor array of claim 16 ~~in which~~ wherein each active-pixel ~~has~~ comprises a row select transistor coupled between said second terminal of said reset transistor and said first input of said amplifier.

5 19. The CMOS-image sensor array of claim 18 ~~in which~~ wherein each active-pixel ~~has~~ further comprises a source follower transistor coupled between said second terminal of said reset transistor and a terminal of said row select transistor.

20. The CMOS-image sensor array of claim 16 ~~in which~~ wherein said first circuit  
10 ~~in of each active-pixel is~~ comprises a photocircuit.

21. The CMOS-image sensor array of claim 20 ~~in which~~ wherein said amplifier comprises ~~is a differential amplifier including in which said first input of said differential amplifier is applied to a first differential amplifier input transistor~~  
15 connected to receive said first amplifier input and ~~said second input of said differential amplifier is applied to a second differential amplifier input transistor~~  
connected to receive said second amplifier input, said first and second differential amplifier input transistors connected ~~cooperating~~ to provide a current signal to a current mirror circuit that is ~~which provides~~ connected to deliver said negative  
20 feedback signal to said reset transistor first terminal.

22. The CMOS-image sensor array of claim 20 ~~in which~~ wherein said photocircuit ~~in of each active pixel includes~~ comprises a photodiode and a capacitance.

25 23. The CMOS-image sensor array of claim 19 ~~in which~~ wherein each said first circuit ~~is~~ comprises a photocircuit.

24. The CMOS-image sensor array of claim 23 ~~in which~~ wherein each said photocircuit ~~includes~~ comprises a photodiode and a capacitance. —

25. A CMOS-image sensor array having rows and columns of active-pixels,  
5 comprising:

~~one or more~~ at least one row lines;

~~multiple~~ a plurality of active-pixels each having an output, the outputs of each active-pixels in a row being connected to a common respective row line, each said active-pixel including:

10 a first circuit that produces a current proportional to incident light intensity, said first circuit being connected to supply said proportional current ~~capable of being applied~~ to said active-pixel output, and

a reset transistor for resetting said active-pixel;

~~one or more~~ at least one amplifiers, each said amplifier having a first input  
15 coupled to ~~a each~~ at least one said row line, - each said amplifier providing being connected to provide a negative feedback signal to each said pixel reset transistor of ~~said a~~ respective row ~~if pixels~~; and,

-a reset reference voltage source connected to apply a reset reference voltage signal to each ~~applied to~~ said amplifier to provide a voltage reference ~~to for~~  
20 controlling reset of said active-pixels.

26. The CMOS-image sensor of claim 25 ~~in which~~ wherein said amplifier further includes a second input for receiving said reset reference voltage signal.

25 27. The CMOS-image sensor of claim 26 ~~in which~~ wherein said reset transistor ~~has~~ includes a gate and first and second terminals, -said first terminal connected to receive

said negative feedback signal ~~provided to said first terminal to adjust the voltage at~~  
said second terminal's voltage ~~of said reset transistor to a~~ selected reset voltage.

28. The CMOS image sensor of claim ~~25 or 27 in which~~ wherein said reset  
5 reference voltage source signal is selected to control said voltage at said second at  
~~each said second terminal is to be about~~  $V_T - \Delta V$  below ~~the a~~ a reset voltage applied at  
said gate terminal of said reset transistor, where ~~where~~  $V_T$  is ~~the a~~ a threshold voltage  
that is characteristic of said reset transistor, and  $\Delta V$  is selected to maintain ~~keeps the~~  
10 said reset transistor in the a subthreshold region of operation during in the a steady  
state phase of of the pixel reset phase.

29. The CMOS image sensor array of claim 27 ~~in which~~ wherein said selected  $\Delta V$   
is greater than about one hundred millivolts.

15 30. The CMOS image sensor array of claim 28 ~~in which~~ wherein each active-pixel  
~~has~~ comprises a column select transistor coupled between said second terminal of said  
reset transistor and said first input of said amplifier.

31. The CMOS image sensor array of claim 30 ~~in which~~ wherein each active-pixel  
20 further comprises ~~has~~ a source follower transistor coupled between said second  
terminal of said reset transistor and a terminal of said column select transistor.

32. The CMOS image sensor array of claim 28 ~~in which~~ wherein said first circuit  
in of each active-pixel is comprises a photocircuit.

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33. The CMOS image sensor array of claim 32 ~~in which~~ wherein said amplifier is  
comprises a differential amplifier including in which ~~said first input of said~~



~~differential amplifier is applied to a first differential amplifier input transistor connected to receive said first amplifier input and said second input of said differential amplifier is applied to a second differential amplifier input transistor connected to receive said second amplifier input, said first and second differential amplifier input transistors cooperating~~ connected to provide a current signal to a current mirror circuit that is which provides connected to deliver said negative feedback signal to said reset transistor first terminal.

34. The CMOS-image sensor array of claim 32 ~~in which wherein~~ said photocircuit in of each active pixel includes comprises a photodiode and a capacitance.

35. The CMOS-image sensor array of claim 31 ~~in which wherein~~ each said first circuit comprises is a photocircuit.

36. The CMOS-image sensor array of claim 35 ~~in which wherein~~ each said photocircuit includes comprises a photodiode and a capacitance.